

Izabella Krucińska,
Wiesława Urbaniak-Domagala,
Magdalena Skoneczna,
*Piero Cosseddu,
*Annalisa Bonfiglio

Possibility of the Application of Low Temperature Plasma for the Deposition of a Polypyrrole Insulating Layer to Construct a Textile-Based Organic Field Effect Transistor

Technical University of Lodz,
Faculty of Material Technologies
and Textile Design,
Department of Fibre Physics and Textile Metrology,
Centre of Advanced Technologies
of Human-friendly Textiles "Pro Humano Tex"
ul. Zeromskiego 116, 90-924 Łódź, Poland,

*Department of Electrical
and Electronic Engineering (DIEE),
University of Cagliari Piazza d'Armi,
09123 Cagliari, Italy, and

INFM-CNR,
Via Campi 213/A, 41100 Modena, Italy

Abstract

The aim of the study was to demonstrate the idea of using the low temperature plasma technique for depositing a thin flexible polypyrrole insulating layer on a Cu monofilament, which plays the role of the gate in a fibrous organic thin film transistor. The active layer was composed of pentacene deposited using the thermal sublimation method. The main focus of the research was the selection of the plasma process conditions, such as the time of deposition, the pressure of polymer vapour as well as the power needed to guarantee the optimal thickness of the layer, its smoothness and uniformity. The characteristics of the drain current - drain voltage obtained for the optimal thickness of the polypyrrole electro-insulating layer - in the range of 0.56-0.88 μm indicate a good field effect, expressed in the modulation of the drain current by the gate voltage and limited value of the leakage current. The results obtained for a cylindrical transistor are comparable to the classical planar OFET's.

Key words: textile transistor; polypyrrole layer; low-temperature plasma.

electronic devices in a fibrous form. The last concept is much more challenging than the first, but such an approach can result in the total unification of electronic devices and systems with apparel. This aspect is very important for the comfort created by e-textiles for the end user.

One of the basic blocks for the development of e-textiles is the study of transistors made from materials suitable to be assembled in the form of a fibre [5]. This idea can be realised using organic semiconductors [6 - 7] because they have unique properties in terms of processability and mechanical properties; with these materials it is possible to construct Organic Thin Film Transistors (OTFT). The first report on OTFT's was published in 1986 [8], and the beginning of this kind of electronic device is closely connected with the discovery of conductive polymers by Shirakawa [9]. Roughly speaking, organic semiconductors are characterised by the electrical properties of semiconductors and the mechanical properties of plastics (even if their electronic properties are much worse than those of inorganic crystalline semiconductors), therefore they are good materials for realising flexible electronic devices using surface engineering technologies. The deposition of a thin film organic semiconductor and dielectric layers is mainly performed by high vacuum deposition [10], thermal evaporation [11], spin-coating [12], or dip coating [13]. To create

deposition, insoluble substances, mainly small molecules and oligomers, are used, for instance, oligothiophene and oligofluorene derivatives [12, 14 - 17], metallophthalocyanines [18 - 19] and acenes [20 - 24] (pentacene, tetracene). For soluble substances the techniques of spin coating and dip coating are used. By using the solution method, good results are achieved in the case of regioregular poly (3-hexylthiophene) [25 - 27]. To realise the patterning process, the following techniques are mostly used: optical lithography, screen-printing, ink-jet printing or soft lithography [12].

Organic transistors have the typical architecture of a thin-film transistor (TFTs), as shown in **Figure 1**.

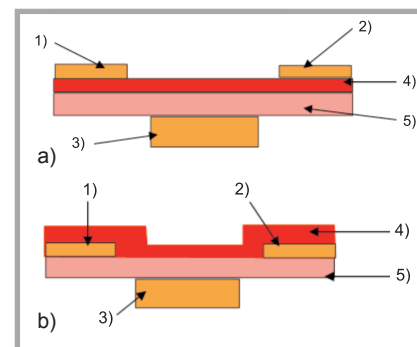


Figure 1. TFT architecture: a) top contact, b) bottom contact (acc. to [12]); 1) source, 2) drain, 3) gate, 4) semiconductor, 5) insulator.

Introduction

During the last decade, the intensive development of e-textiles has been observed. The term "e-textile" refers to fibrous products with incorporated electronics. As a matter of fact, in terms of structure, they can be divided into two groups: The first group of products, currently very well developed and commercially available, consist of miniaturised electronic devices obtained by embedding classical silicon technologies into a textile substrate [1 - 4]. The second group of products, which is still in its embryonic phase, consists of devices that have a textile structure, i.e.

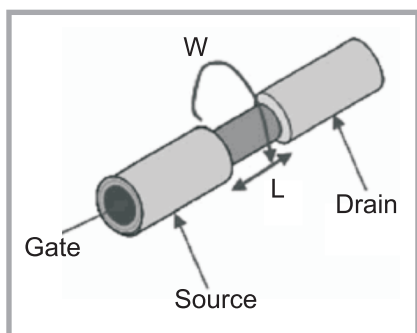


Figure 2. Scheme of a field effect transistor on a fibre (acc. to [7]).

The “bottom contact” architecture was used by Bonfiglio et al. [11] to produce flexible organic thin film transistors (OTFT) based on a flexible insulation layer, which, after assembling the source, drain, gate and semiconductor, can be transferred onto flexible substrates such as textiles. In a further development [6], this concept was used for developing a dedicated OTFT architecture for textile applications. This new structure is obtained by laminating the structure of an organic thin film transistor on a textile ribbon. In this case the top contact TFT architecture was employed. The insulating layer is composed of a polyethylene terephthalate film (Mylar™) characterised by suitable dielectric properties (a dielectric constant equal to 3.0 and a thickness of 900 nm). The gate metal layer (gold or aluminium) was made using the evaporation technique. Three different semiconductor layers were investigated. In two cases these layers were deposited using the drop casting method from a solution of regioregular poly-3-exil-thiophene or regioregular 3,3-didocel-2, 2:5,2-terthophene. In the third variant the evaporation technique for pentacene was used. The transistor yarns thus developed were implemented into woven structures as the weft, whereas for the warp two kinds of metallic yarns were implemented acting as a source and drain, keeping close contact with the outer layer of transistor yarns i.e. with the organic semiconductor layer.

An alternative option for realising OTFT's in a textile form is to use cylindrical geometry. In this case the top-contact configuration is the most suitable. According to the idea presented by Maccioni *et.al.* [7], a metallic, flexible, cylindrical wire is used as a mechanical base for the transistor and as its gate. As a gate insulator, a thin insulating layer must be deposited on the metallic wire; the main

requirements for the insulating layer are a high breakdown voltage and extremely low conductivity. The next layer is an organic semiconductor layer, on top of which the electro-conductive source and drain electrodes should be deposited. The localisation of electrodes can be done using a mechanical mask. The critical point is to control the gap between electrodes properly. The scheme of a field transistor on a fibre is presented in **Figure 2**.

The goal of the present paper is to demonstrate potential technology for the deposition of an electro-insulating layer on a copper monofilament to make an organic thin film transistor in a fibrous form. From among the potential methods used in surface engineering, the low temperature plasma method was selected. A low temperature plasma pyrrole environment was generated to develop the insulating layer on a copper gate, taking the form of a monofilament.

Materials for textile transistors

Copper monofilaments with a diameter of 0.61 mm were used as a gate in the fibrous transistor. For the deposition of the thin insulating layer, pyrrole obtained from Sigma-Aldrich, with a purity of 98%, freshly distilled under a vacuum and stored at a temperature of $-4\text{ }^{\circ}\text{C}$, was used. The active layer was formed using p-type semiconductor pentacene. Source and drain contacts were formed from poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) - a conductive polymer that was deposited on top of the semiconductor layer by means of a poly(dimethylsiloxane) (PDMS) rubber stamp whose surface was patterned with the geometry of the contacts.

Methods

Deposition of the insulating layer by the plasma method

The deposition of the electro-insulating polymer layer on the gate was carried out using a low-temperature plasma reactor system, which consisted of a glass cylindrical chamber of 10 cm diameter and 70 cm length with a coil outside powered by a matching box. A low temperature plasma monomer environment was generated by means of a RF field with a frequency of 13.56 MHz. An electrodeless discharge, type H, was used, and the high frequency generator applied

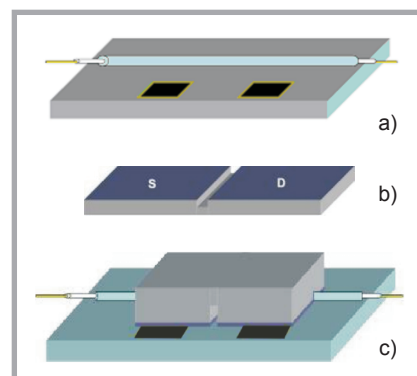


Figure 3. Method of manufacturing an OTFT to inspect the quality of the insulating layer: a) deposition of a pentacene layer on the substrate, b) manufacturing the drain and source, c) assembling the OTFT investigated.

allowed to control the power within the range of 0 - 300 W. The construction of the flow reactor enabled vacuum adjustment from 0.133 Pa to 133 Pa. The gas pressure in the reactor was measured by means of a resistance probe, and a PN-21 vacuum meter from Unitron-Unima was also used. The pressure of gases was measured in a stationary flow state of the monomer vapour immediately prior to switching on the generator and discharge initiation. The ampoule containing liquid pyrrole connected to the vacuum line was cooled to a temperature of $0\text{ }^{\circ}\text{C}$. The vapour of toxic compounds developed during the synthesis of polypyrrole was arrested in a cold trap located in front of the vacuum pump. In order to cover the gate of the fibrous transistor, the copper monofilament was centrally placed along the axis of the glass carrier in the reactor. In the first step, the surface of the Cu monofilament was cleaned and activated in argon plasma for 30 min with an effective applied power of 100 W. Then the argon gas flow was switched off and pyrrole vapour introduced.

The adjustment of the values of technological parameters for each variant of the sample was based on the results presented in [27]. Urbaniak *et.al.* indicated that the layer thickness deposited using a low-temperature plasma pyrrole environment generated by means of a RF field with a frequency of 13.56 MHz is a linear function of the deposition time. The plasma polypyrrole deposition rate increases with a rise in the pressure of the monomer vapour. To guarantee a high quality of the insulating layer in OTFT's, two parameters are very important: the optimal thickness of the insulating layer, and its smoothness

Table 1. Results of the plasma deposition of the insulating layer:

Sample	Effective power, W	Time of deposition, min	Pressure of monomer vapour, Pa	Thickness, μm
Variant 1 pPPy	8	10	8.0	0.32 - 0.46
Variant 2 pPPy	8	15	8.0	0.56 - 0.88
Variant 3 pPPy	8	30	8.0	1.03 - 1.17
Variant 4 pPPy	25	20	13.33	2.45 - 2.47

and continuity around the whole monofilament. Therefore the values of the technological parameters of the plasma deposition were adjusted to change the thickness and character of the deposited layer. The thickness of the polypyrrole layers was controlled thanks to the selection of three different sets of techno-

logical parameters i.e. the power, time, and monomer plasma densities resulting from the different pressures of the monomer vapour. The time was changed within the range of 10 - 30 min, and the effective power was set at 8 W and 25 W. The pressure of monomer vapour was changed within the range of 8 to 13.3 Pa.

Methods for the inspection of the quality of the insulating layer

In order to facilitate the measurement of the transistor performance (an indirect indication of the insulating layer quality), the soft lithographic lamination technique was employed to connect the source and drain electrodes. The procedure employed is reported as follows, step by step:

- two gold pads were deposited on a glass substrate,
- the Cu-pPPy monofilament was fixed onto the glass substrate, and a thin pentacene layer was deposited by thermal sublimation (*Figure 3.a*),

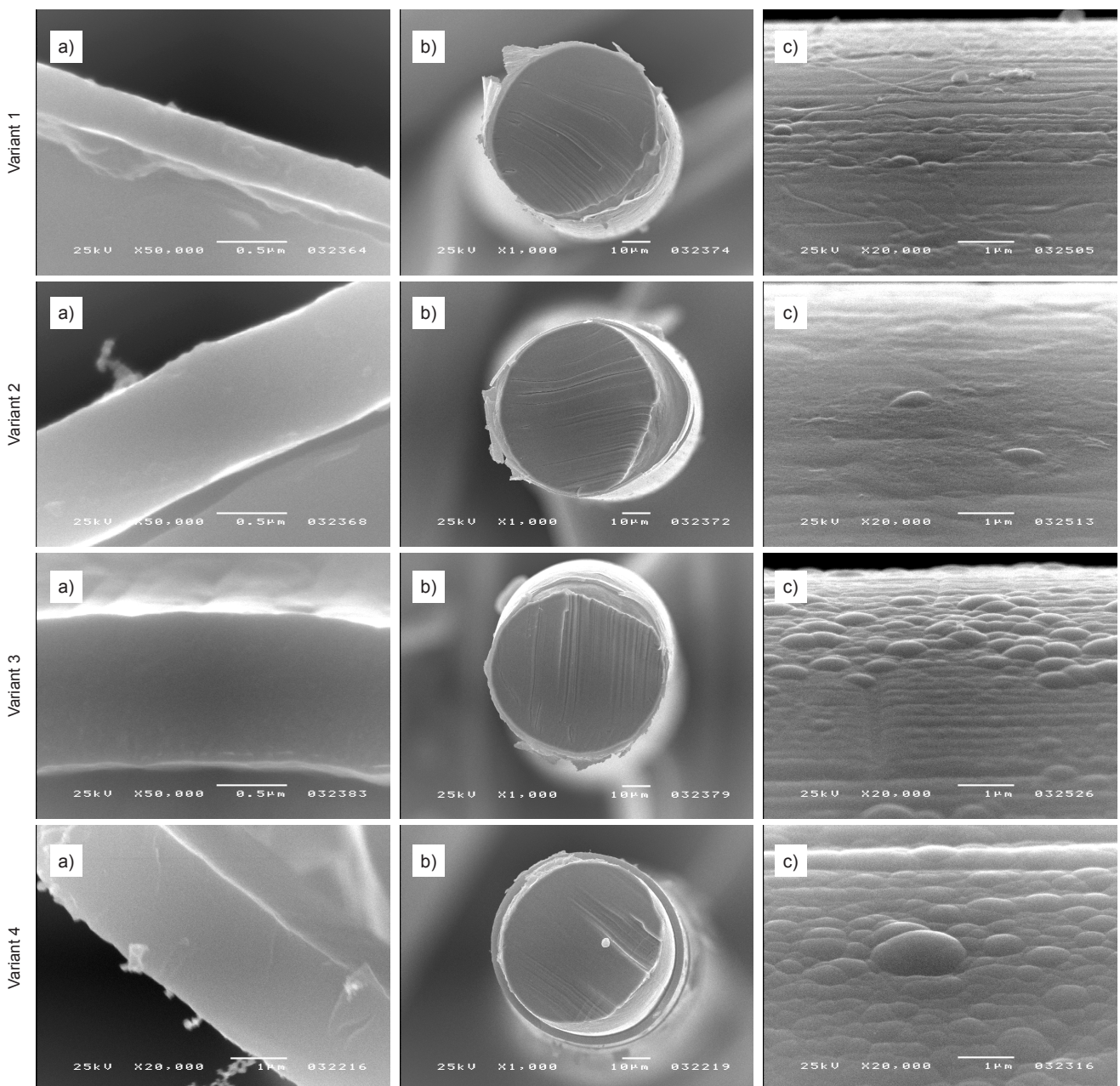


Figure 4. Surfaces of Cu wire coated with plasma polypyrrole for variant 1, 2, 3 and 4: a) cross-section of the insulating layer, b) cross-section view of Cu wire covered with polypyrrole, c) longitudinal view of the insulating layer.

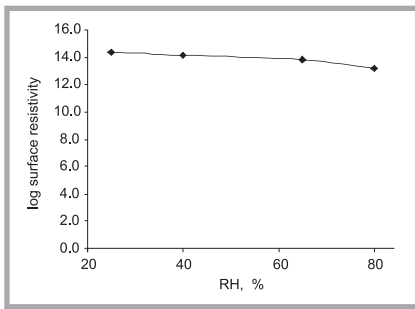


Figure 5. Electric resistivity properties of the plasma polypyrrole layer.

- a poly(dimethylsiloxane) (PDMS) rubber stamp was used to print the source and drain contacts on the monofilament surface. The PDMS surface is previously coated with a conductive polymer-poly(3,4-ethylenedioxythiophene): poly(styrene sulfonate) (PEDOT:PSS) deposited by spin coating (**Figure 3.b**),
- the rubber stamp was brought into contact with both the monofilament surface and the gold pads previously deposited (**Figure 3.c**).

Based on such a procedure, key measurements of the performance of the transistor developed were made. The capacitance of the insulating layer per unit area was calculated according to the formula:

$$C_i = \frac{\epsilon_i}{r_i \ln \left(\frac{r_i}{r_g} \right)} \quad (1)$$

where:

- ϵ_i - dielectric permittivity of the insulator,
- r_i - radius of the copper monofilament covered by a polypyrrole layer,
- r_g - radius of the copper monofilament.

The current-voltage characteristics were determined using a HP4155 semiconductor parameter analyser.

Based on the measurement of the current-voltage characteristics, the carrier mobility was determined. Carrier mobility, μ , describes how easily charge carriers can move within the semi conductive layers under the influence of an electrical field. For typical amorphous Si layers, these parameters take a value in the range of 0.1 - 1 cm²/Vs [12]. The next important parameters determined on the basis of current-voltage measurements is the ratio of the drain current in an on state to the current in an off state - I_{on}/I_{off} . A low current in the off state is desired to eliminate the leakage current while in an inactive state; therefore the ratio of currents should be as high as possible. According to literature [12], a ratio as high as 10⁶ can be achieved by OTFT's.

Results

Results related to the deposition of the insulating layer

The surface morphology and cross-section of the plasma polypyrrole layers was assessed by means of a scanning microscope - JEOL JSM-5500 SEM. The thickness of the film covering the gate was determined by analysing images of cross-sections of the layers. The cross-sections were prepared in two ways: by means of a blade at room temperature or by fracturing after prior cooling in liquid nitrogen. The observations were made at an accelerating voltage of 10 kV and magnifications from 1000× to 50000×. To obtain a suitable insulating layer on the Cu wire, several tests were carried out using different technological parameters.

In this paper only some variants of the optimal layers for electronic purposes were discussed.

The results of the measurement of the thickness of the plasma deposited lay-

ers are given in **Table 1** and illustrated in **Figures 4**.

Figures 4 show that the polypyrrole uniformly covers the whole surface of the Cu monofilament. The surface smoothness is a function of the monomer vapour pressure, which in turn, as known from [27], is a function of the deposition rate. At a pressure of 13.3 Pa, the rate of layer formation is equal to 74 $\mu\text{m min}^{-1}$, and when the pressure decreases to 8 Pa, this rate amounts to 33 $\mu\text{m min}^{-1}$ [27]. This means that for all the variants obtained at a pressure of 8 Pa, the thinnest layers were attained for the shortest time of plasma deposition. The lower rate of layer formation resulted in covering the monofilament with a layer characterised by a smooth surface (**Figure 4 variant 1.c**). After the application of a higher rate of layer formation, granular bump-like structures were observed on the top layer (**Figure 4 variant 4.c**).

Results of the inspection of the quality of the insulating layer

Polypyrrole plasma layers deposited on Cu wire are characterised by a light yellow colour (polymer colour remains unchanged for many years); the layers are hard and cross-linked by the UV component. The electro-insulating properties of the layers were tested in an environment with various quantities of water vapour that show small changes in the electric resistivity of the layers (**Figure 5**).

The lamination technique employed allowed to easily obtain stable contact during the characterisation of the electrical devices. As can be noticed, the devices worked perfectly as unipolar p-type OFET's in the accumulation regime. The current-voltage characteristics obtained for the optimal variants are given in **Figures 6** and **7**.

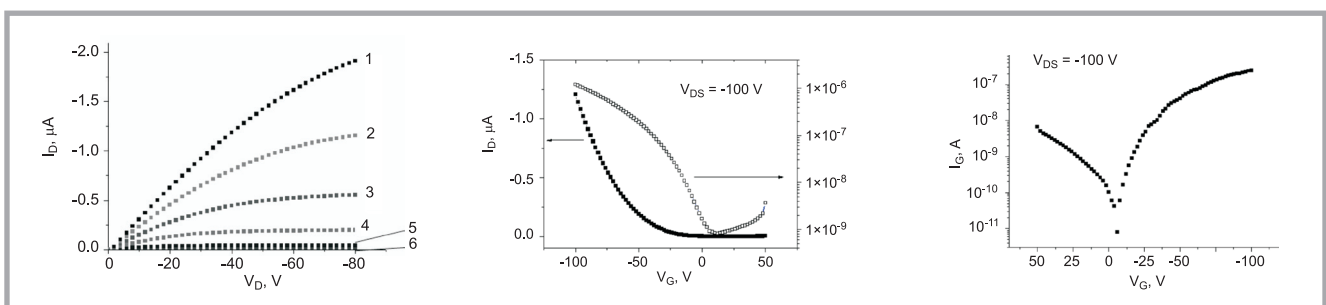


Figure 6. Current-voltage characteristics for variant 2; 1) $V_g = -100\text{ V}$, 2) $V_g = -80\text{ V}$, 3) $V_g = -60\text{ V}$, 4) $V_g = -40\text{ V}$, 5) $V_g = -20\text{ V}$, 6) $V_g = 0\text{ V}$.

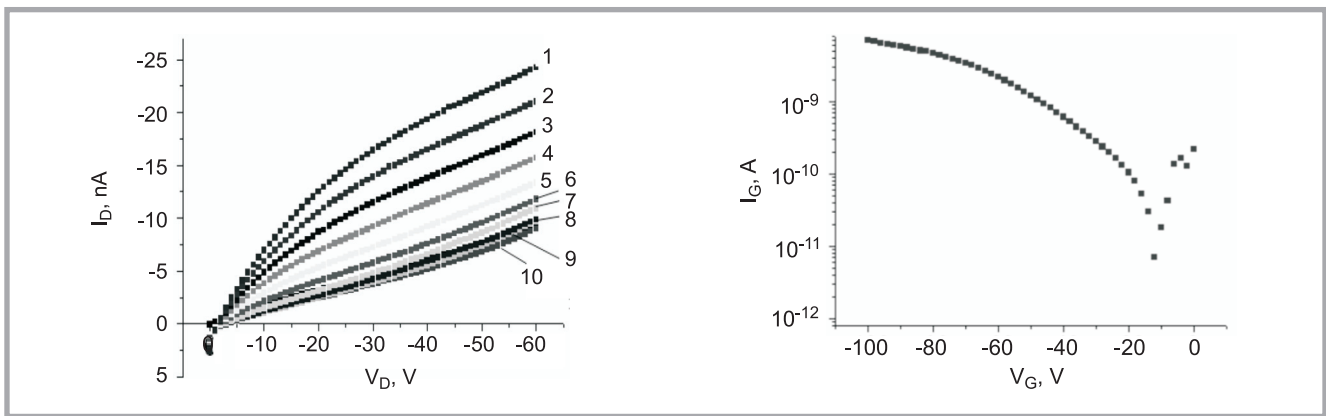


Figure 7. Current-voltage characteristics for variant 3; 1) $V_g = -100$ V, 2) $V_g = -90$ V, 3) $V_g = -80$ V, 4) $V_g = -70$ V, 5) $V_g = -60$ V, 6) $V_g = -50$ V, 7) $V_g = -40$ V, 8) $V_g = -30$ V, 9) $V_g = -20$ V, 10) $V_g = 0$ V.

For the devices constructed using a Cu monofilament covered by an insulating layer according to the conditions adjusted in variant 1, a huge value of the leakage current (I_g) was obtained, and, as a consequence, the transistor did not work. Probably, in these conditions the insulating layer is too thin to guarantee good insulation properties. Much better results were obtained for variant 2 (Figure 6). The characteristics of the current-drain voltage indicate a good field effect i.e. a good modulation of the drain current by the gate voltage; the leakage current is rather limited. For this variant, considering that $C_{ins} = 1\text{ nF/cm}^2$ and $W/L = 1$, the following values of transistor parameters were obtained: a mobility up to $6.65 \times 10^{-1} \text{ cm}^2/\text{Vs}$, V_{th} up to -16 V and I_{on}/I_{off} up to 2.6×10^3 . To check the reproducibility of the device performance for the same monofilament, other devices were fabricated using the same methodology (It is totally unnecessary to show similar curves again). As a result, a good reproducibility of the current-voltage characteristics was obtained in all cases.

In Figure 7, the results obtained for variant 3 are reported. In this case, considering $C_{ins} = 1\text{ nF/cm}^2$ and $W/L = 1$, a mobility up to $1 \times 10^{-2} \text{ cm}^2/\text{Vs}$ was obtained; the V_{th} is equal to -2.4 V and the I_{on}/I_{off} amounts to 2.6. A weak field effect was obtained despite very low levels of leakage current. A possible reason for this behaviour can be a too high thickness of the insulating layer, which on one hand reduces the leakage current (positive effect) but on the other decreases the capacitance value of the dielectric and, as a consequence, the effect of the gate voltage on the device performance (negative effect).

Similar results were obtained for variant 4, characterised by an insulating layer of the greatest thickness from all the samples (more than 2 μm). Also in this case (data not shown) the insulating film deposited was too thick to allow good field effect behaviour, while a high thickness of the deposited insulating layer caused low leakage currents.

Before the application of a cylindrical organic thin film transistor in textiles, the transistor created should be protected by a polytetrafluoroethylene layer [26].

Conclusions

This study has demonstrated the idea of the using low temperature plasma technique for obtaining thin polypyrrole insulating layers on a Cu monofilament, which plays the role of the gate in a cylindrical organic thin film transistor. The active layer was composed of pentacene deposited using the thermal sublimation method. The main research was focused on the selection of the plasma process conditions, such as the time of deposition, the pressure of polymer vapour as well as the effective power to guarantee an optimal thickness of the layer, its smoothness and uniformity. The results presented allow to define the following conditions: First the SEM images of the surfaces and cross-sections of the plasma polypyrrole layers indicate that the application of a symmetric sample arrangement in the reactor and an electrodeless charge with a field frequency of 13.56 MHz and effective power of 8 and 25 W resulted in a uniform deposition of plasma layers around the whole cylindrical surface. The smoothness of the outer surface of the layers is a function of the monomer vapour pressure. A smooth surface was obtained by applying

a pressure of 8 Pa, but when the pressure was increased to 13.3 Pa, granular bump-like structures developed on the top layer. The thickness of the electro-insulating layer is a function of the deposition time of pyrrole vapour. A longer time of deposition causes the formation of a thicker layer. Analysis of the current-voltage characteristics of the devices indicates that the proper action of OTFT's depends on the thickness of the polypyrrole insulating layer. An OTFT with a polypyrrole electro-insulating layer of $0.32 - 0.46 \mu\text{m}$ thickness is characterised by a huge value of the leakage current (I_g). For OTFT's with polypyrrole layers of a thickness greater than $1 \mu\text{m}$, no field effect and very low levels of leakage current were obtained. A too high thickness reduces the capacitance value of the dielectric and, as a consequence, the effect of the gate voltage on the device performance (negative effect). An optimal thickness of the polypyrrole electro-insulating layer, within the range of $0.56 - 0.88 \mu\text{m}$, was obtained for technological variant 2 (effective power - 8 W, pressure of monomer vapour - 8 Pa, and time of deposition - 15 min). The characteristics of the drain current-drain voltage obtained for this variant indicates a good field effect and, at the same time, a rather limited leakage current. For this variant, considering that $C_{ins} = 1\text{ nF/cm}^2$ and $W/L = 1$, the following values of transistor parameters were obtained: a mobility up to $6.6 \times 10^{-1} \text{ cm}^2/\text{Vs}$, V_{th} up to -16 V and I_{on}/I_{off} up to 2.6×10^3 . Analysis of the current-voltage characteristics for all the devices constructed using a variant 2 monofilament shows the reasonable reproducibility of all the transistor parameters determined.

Acknowledgments

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90-570 Łódź, Poland;
Phone: (48-42) 638-03-68, Fax: (48-42) 637-65-01
E-mail: dariusz.wawro@ibwch.lodz.pl